

UNITED STATE EPARTMENT OF COMMERCE Patent and Trademark Office

Address: COMMISSIONER OF PATENTS AND TRADEMARKS Washington, D.C. 20231

APPLICATION NO.	FILING DATE		FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/931,125	09/16/97	LEE	Н	P54508

LM51/1207

ROBERT E BUSHNELL 1522 K STREET, N.W. SUITE 300 WASHINGTON DC 20005-1202 EXAMINER PORTKA, G

ART UNIT PAPER NUMBER 2759

DATE MAILED: 12/07/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No. 08/931,125

Applicant(s)

Lee

Examiner

Gary J. Portka

Group Art Unit 2759



Responsive to communication(s) filed on Sep 20, 1999				
∑ This action is FINAL.				
☐ Since this application is in condition for allowance except for formal matters in accordance with the practice under Ex parte Quay#835 C.D. 11; 453 O.				
A shortened statutory period for response to this action is set to expire longer, from the mailing date of this communication. Failure to respond within application to become abandoned. (35 U.S.C. § 133). Extensions of time may 37 CFR 1.136(a).	the period for response will cause the			
Disposition of Claim				
X Claim(s) <u>1-6</u>	is/are pending in the applicat			
Of the above, claim(s)	is/are withdrawn from consideration			
Claim(s)	is/are allowed.			
	is/are rejected.			
Claim(s)	is/are objected to.			
☐ Claims	are subject to restriction or election requirement.			
See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948. ☐ The drawing(s) filed on				
Attachment(s) X Notice of References Cited, PTO-892				
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). ☐ Interview Summary, PTO-413 ☐ Notice of Draftsperson's Patent Drawing Review, PTO-948 ☐ Notice of Informal Patent Application, PTO-152	<u> </u>			
SEE OFFICE ACTION ON THE FOLLOWING PAGES				

Art Unit: 2759

DETAILED ACTION

1. Claims 1-6 have been amended by Applicant, and are presented for examination.

Drawings

- 2. The drawings are objected to because:
- a. Applicant has disputed that Figures 1 and 3 should be labeled "Prior Art" and instead labeled them "Related Art". This labeling should be removed because it is not sanctioned by the MPEP and only confuses the issue.

Claim Objections

- 3. The disclosure is objected to because of the following informalities:
 - a. In claim 1 at line 5, it is suggested to insert --of-- before "memory devices".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 6 recites at lines 14-21 that if parity misses the cache, the cache is updated, and if not, the cache is not updated. This is counter to the description which states at pages 11-12 that in

Art Unit: 2759

either case the cache table gets updated. As shown in Figure 5, in either case the cache gets updated; thus it appears from the disclosure that Applicant intends updating the cache table to be equivalent to updating the cache.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to

particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites at lines 14-21 that if parity misses the cache, the cache is updated, and if not, the

cache is not updated; further it states that the cache table is updated. Depending upon whether

Applicant intends updating a cache table to be equivalent to updating a cache, it is not clear if

"updating a cache table" at line 21 occurs always (whether or not the cache was updated as described

at lines 16 or 18), or if parity hits in the cache, since the cache is not updated, this updating of the

cache table is skipped.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness

rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Art Unit: 2759

9. Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones, U.S.

Patent 5,572,660.

10. As to claim 1, Jones discloses a memory system comprising:

a. Plurality of defect-adaptive devices (214) as claimed, a first region storing information

needed for data recovery in disk drive 214-8, and a second region storing data in disk drives 214-1

through 214-7 (see Abstract and front page figure);

b. Plurality of caches (212 and 213) respectively connected to the devices, a cache (213)

for storing information blocks needed for data recovery (see Abstract and front page figure; since the

array scheduler schedule accesses to the drives, information blocks are read from a predetermined

memory device as claimed);

c. Controller (210) connected to each device and cache, controlling writing and reading,

and obtaining information needed for data recovery from a memory device (214-8), and storing that

information in a predetermined cache 213 (see Abstract; also see column 2 line 62 to column 4 line

6, in particular column 3 lines 30-39).

In the embodiment referred to above, Jones does not disclose the plurality of caches storing

the information needed for data recovery (instead teaching one cache for this, 213), and does not

disclose reading, writing, and obtaining the information needed for data recovery from each memory

device (instead teaching from one memory device, 214-8). However, Jones states at column 3 lines

15-18 that a similar write-back caching scheme for parity may be used for a RAID-5 system. At

column 2 lines 46-53, it is taught that distributing the parity across the disk drives as in RAID-5

P

Art Unit: 2759

improves write throughput, thus motivating an artisan to attempt to implement the method of Jones in RAID-5. In such an implementation, each of the memory devices store parity, and since each device is associated with a cache, so do each of the caches. (Note that this spreads the recited first and second regions across the disk drives.) Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to store and access information needed for data recovery (parity) on each disk drive, and as a result in the plurality of caches, because this distributes parity across the device, which improves write throughput as taught by Jones.

- 11. As to claim 2, Jones discloses that the controller determines if the information needed for data recovery is in the cache (see Figure 3D item 344, and Figure 3E item 370).
- 12. As to claim 6, Jones discloses a RAID system comprising:
- a. Plurality of disk drives (214) storing data blocks and parity information (see Abstract and front page figure);
- b. Plurality of caches (212 and 213), one (213) storing parity information (see Abstract and front page figure);
- c. Controller (210) connected to each disk drive and cache controlling write of data and parity by:
- i. Calculating target location on disk upon receiving write instruction (see Figure
 3A items 308 and 330);
 - ii. Reading old data from the disk (see Figure 3C item 360);

Art Unit: 2759

iii. If old parity to be read from disk is not in the cache, reading the old parity, and updating the cache; or if hit in the cache not updating the cache (to the extend disclosed and understood; see Figure 3E items 370, 376-378, and Figure 3F item 392);

- iv. Obtaining new parity by performing XOR between old parity and new data (see Figure 3F item 390, and column 9 line 16 equation);
- v. Writing the new data and new parity on the target location (see Figure 3F item 394, and column 3 lines 25-40).

Jones does not specifically disclose that each disk drive stores data and parity in the preferred embodiment. However, Jones states at column 3 lines 15-18 that a similar write-back caching scheme for parity may be used for a RAID-5 system. At column 2 lines 46-53, it is taught that distributing the parity across the disk drives as in RAID-5 improves write throughput, thus motivating an artisan to attempt to implement the method of Jones in RAID-5. In such an implementation, each of the memory devices store data and parity. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to store data and parity on each disk drive, because this distributes parity across the device, which improves write throughput as taught by Jones.

- 13. Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones, U.S. Patent 5,572,660 and Seki, U.S. Patent 5,809,206.
- 14. As to claim 3, Jones does not disclose that the information needed for data recovery is sequentially arranged from the most outer cylinder. However, it is well known that the sequential nature of disk access invites a transfer mechanism sequentially from some position. As taught by

Art Unit: 2759

Seki, arranging data and error correction code (information needed for data recovery) from the outer track to the inner track is desirable to reduce access time by minimizing seek time (see column 10 lines 40-47 and column 13 lines 48-51). The example of error correction data at the outer track is specifically disclosed at column 10 lines 61-65 and column 13 lines 52-57. The advantage of faster access due to reduced seek time would have motivated an artisan to arrange this information from the outermost cylinder. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to sequentially arrange the recovery information from the most outer cylinder in Jones, because as taught by Seki this method reduces seeking time and therefore improves performance..

- 15. As to claim 4, Jones discloses that information needed for data recovery is modified to a value obtained through a calculation of new data recovery information (see column 9 lines 8-21).
- 16. As to claim 5, Jones discloses XORing of previous data, previous recovery information, and new data (see column 9 line 16 equation).

Response to Arguments

17. Applicant's arguments filed September 20, 1999 have been fully considered but they are not persuasive.

Applicant has argued that Jones does not teach that data and parity are written in the same disk drive. This was not specifically recited originally in claim 1. Claim 1 originally stated "controlling reading and writing of data and information needed for data recovery in each memory device", in which "data and information" may be grouped as desired to cover "each device", and not

Art Unit: 2759

necessarily interpreted as "data in each device" and "information in each device". The amended claim states "information in each device", which necessitates the new grounds of rejection, basically as was applied to claim 6 previously.

Applicant has argued that Jones does not teach that only parity information is written in a cache. This argument is not supported by the claim language.

Applicant has disputed Examiner's previous Official Notice that information needed for data recovery is well known and desirable to arrange from the outermost cylinder. In response, a reference has been provided to substitute for the original Official Notice in the 35 U.S.C. 103 rejection above.

Applicant has argued with regard to claim 6 that there is no teaching or suggestion in Jones to perform the modification, that hindsight has been used, and that distributing parity across the disks as in RAID-5 does not result in obviousness to store data and parity on each disk drive. Examiner disagrees with all of these statements. The sections cited in Jones clearly convey to an artisan that a variation of the disclosed embodiment is in a RAID-5 implementation, and provides the teaching of why this may be desirable. Such an implementation stores data and parity on each disk drive as claimed.

Conclusion

18. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the

Art Unit: 2759

THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

19. Any response to this final action should be mailed to:

Box AF Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703) 308-9051, (for formal communications, please mark "EXPEDITED PROCEDURE")

or:

(703) 308-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

20. Any inquiry concerning this communication from the Examiner should be directed to Gary J. Portka at telephone number (703) 305-4033. The Examiner can normally be reached on weekdays from 9:00 A.M. to 5:30 P.M.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Do Yoo, can be reached on (703) 308-4908. The fax phone number for this Group is (703) 308-9731.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, whose telephone number is (703) 305-3900.

GJP

Gary J. Portka

Patent Examiner

November 23, 1999

Do Hyun Yoo
Primary Examiner